Directory structure

Root\fpt2011_design\src\rtl\verilog : RTL verilog files

Root\fpt2011_design\src\tb\verilog : Testbench verilog files

Root\fpt2011_design\syn\connect6 : Synthesise directory

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connect6.xise - Xilinx ISE -13.2 project file
connect6_s3.ucf - User constraints file for Spartan-3A evaluation board
connect6_s6.ucf - User constraints file for Atlys evaluation board
connect6_s3.bit - Bitstream for Spartan-3A FPGA configuration
connect6_s3.mcs - File for Spartan-3A flash programming
connect6_s6.bit - Bitstream for Atlys Spartan6 FPGA configuration

Root\fpt2011_design\sim : Simulation directory

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rungui.do - TCL script for Modelsim simulator

Running the simulation

A Tcl/Tk based script makes it possible for human players to compete against the FPGA logic. This was simulated using Modelsim-SE 6.6 simulator, but should be compatible with any version of Modelsim-SE and with slight modifications with PE, DE and XE versions.

1. Open the Modelsim Simulator.
2. Change the current directory to the simulation directory.
3. Execute the command “do rungui.do” at the transcript window.
4. Select the FPGA playing colour by clicking the appropriate radio button.
5. The complete log of the game will be displayed in the transcript window with different colours for user and FPGA movements.
6. Trying to make an illegal move such as placing three stones will lead to termination of the simulation.
7. There is no “undo” option since each move is updated in the internal registers as soon as it occurs.
8. If the FPGA wins, that info is displayed and the simulation terminates. Currently the logic for checking whether the user has won is not added, hence needs to be checked manually.